G2 Bus Restrictions (Hardware) No. 1 Development Department February 18th , 1999

The following are restrictions on hardware that connects to the G2 Bus Expansion Area. This document only covers those restrictions that are relevant to satisfying software restrictions that are described in the counterpart to this document, “G2 Bus Restrictions (Software)”.
Other design restrictions exist, but are not addressed herein. Please contact the No.2 Development Department regarding other restrictions.

Restrictions

(1) Single reads and single writes (1-byte, 2-byte, and 4-byte read and write) over the G2 Bus must take less than 1 μsec. (25 G2 clock cycles)

(2) Burst reads and burst writes (32-byte read and write) over the G2 Bus must take less than 3.4 μsec. (85 G2 clock cycles)

(Note) If the hardware has an internal write buffer, the above conditions must be satisfied when accessing that buffer even if it contains data.

Explanations

(Explanation 1) The Dreamcast internal bus may stop for more than 16 μsec if devices on the G2 bus (G2 Bus control registers, MODEMs, AICA, and G2 Bus Expansion Areas) are accessed without satisfying these conditions. If this overlaps with Maple DMA, acquisition of Maple data may fail.
In the worst case, data in system memory may be lost. (This is because system memory refresh cycles become insufficient and SDRAM specifications (ACT-PRE＜120 μsec) are not satisfied.)

(Explanation 2) Access takes the most time when a CPU burst read occurs while the G2 bus is being accessed by EXT-DMA while the Holly G2i/f Block buffer contains 8 single writes and the SH4i/f Block buffer contains a single burst write. When this happens, the final CPU burst read takes 19890 nsec.
This does not affect Maple because time on the RootBus is divided into segments of less than 16 μsec.??
However, countermeasures are needed nonetheless because this condition prevents system memory from being refreshed. When the above indicated access takes 2 msec, the refresh interval must be 15.161 μsec or less in accordance with expression (a) below. Since the maximum refresh interval under normal circumstances is 15.625 μsec (per expression (b)), this is a reduction of 0.5 μsec.

(16msec - 2msec) / (1024 - (2msec / 19890nsec)) = 15.161 μ sec ･･･(a)
16msec / 1024 = 15.625 μ sec ･･･(b)