G2 Bus Restrictions (Software)

Access to the following areas over the G2 bus is subject to restrictions, both for single and multiple access.

G2 Bus Control Register:	An internal Holly register which controls G2 Bus operation.
MODEM:	An internal register on the modem connected to the extension connector.
AICA:	This includes AICA internal registers (Sound and RTC) and Sound Memory connected to AICA. (DMA is only possible with Sound Memory.)
G2 Bus Expansion Area:	Area for hardware expansion by connection to the extension connector.

The following types of access are possible.

SH4 Program:	access to all areas
SH4 DMA(ch1, ch3):	access to all areas
GD-DMA:	access to AICA Sound Memory and G2 Bus Expansion Area
AICA-DMA:	access to AICA Sound Memory
EXT-DMA1:	access to G2 Bus Expansion Area
EXT-DMA2:	access to G2 Bus Expansion Area

Restrictions on Area Access

(1) Restrictions on G2 Bus Control Register Access

(1.1) G2 Bus Control Register access by program is only allowed using 4-byte access. No other access size is possible.

NG 1byteWR, 1byteRD
NG 2byteWR, 2byteRD
OK 4byteWR, 4byteRD
NG 32byteWR, 32byteRD (occurs when using cache or SQ)

(1.2) SH4 DMA (ch1, ch3) to the G2 Bus Control Registers is inhibited.

(1.3) During GD – DMA (GD => AICA Sound Memory), G2 Bus Control Register access is inhibited. (=> contention 3)

(2) Restrictions on MODEM Access

(2.1) MODEM access by program is restricted to 1-byte access. No other access size is possible.

OK 1byteWR, 1byteRD
NG 2byteWR, 2byteRD
NG 4byteWR, 4byteRD
NG 32byteWR, 32byteRD (occurs when using cache or SQ)

(2.2) SH4 DMA (ch1, ch3) to MODEM is inhibited.

(2.3) During GD–DMA (GD => AICA Sound Memory), MODEM access is inhibited. (=> contention 3)

(3) Restrictions on G2 Bus Expansion Area Access (areas connected to restriction-compliant hardware)

Paragraph (4) below applies if hardware is connected but not enabled.

(3.1) G2 Bus Expansion Areas are accessible by program, regardless of byte size.

OK 1byteWR, 1byteRD
OK 2byteWR, 2byteRD
OK 4byteWR, 4byteRD
OK 32byteWR, 32byteRD (occurs when using cache or SQ)

(3.2) SH4 DMA (ch1, ch3) is possible to the G2 Bus Expansion Area.

(3.3) GD-DMA to the G2 Bus Expansion Area is only possible from GD to the G2 Bus Expansion Area. During this DMA, AICA reads by program are inhibited. (=> contention 4)

OK GD-DMA (GD => G2 Bus Expansion Area)
NG GD-DMA (G2 Bus Expansion Area=> GD) <cannot be set>

(3.4) During GD-DMA (GD => AICA Sound Memory), access to the GD Bus Expansion Area is inhibited. (=> contention 3)

(3.5) EXT-DMA0 and EXT-DMA access is only possible in the "Interruptible Mode". Accordingly, bit 2 of registers E1TSEL and E2TSEL must be set to '1'. (=> reference 3)

During DMA, AICA reads by program are inhibited. (=> contention 5)

(4) Restrictions on G2 Bus Expansion Area Access (areas not connected to hardware)

The following also applies if connected hardware is disabled.

(4.1) G2 Bus Expansion Area access by program is possible using 1-byte, 2-byte and 4-byte access.

32-byte access is inhibited.

OK 1byteWR, 1byteRD
OK 2byteWR, 2byteRD
OK 4byteWR, 4byteRD
NG 32byteWR, 32byteRD (occurs when using cache or SQ)

(4.2) SH4 DMA (ch1, ch3) to the G2 Bus Expansion Area is inhibited.

(4.3) G2 Bus Expansion Area access by GD-DMA is inhibited.

(4.4) During GD-DMA (GD => AICA Sound Memory), G2 Bus Expansion Area access is inhibited. (=> contention 3)

(4.5) G2 Bus Expansion Area access by EXT-DMA0 and EXT-DMA1 is inhibited.

(5) Registration on G2 Bus Expansion Area Access (areas connected to hardware that does not comply with restrictions)

(5.1) Access restrictions depend on hardware.

(6) Restrictions on AICA Access

(6.1) AICA access by program is possible using 4-byte access.

No other access size is possible.

When accessing AICA, it is necessary to confirm that the hardware's write buffer is empty. (=> contentions 1, 2)

NG 1byteWR, 1byteRD
NG 2byteWR, 2byteRD
OK 4byteWR, 4byteRD
NG 32byteWR, 32byteRD (occurs when using cache or SQ)

(6.2) SH4 DMA (ch1, ch3) to AICA is inhibited.

(6.3) GD-DMA to AICA Sound Memory is only possible from GD to AICA Sound Memory.

During DMA to AICA Sound memory, program access to G2 Bus Control Registers, MODEM, AICA and the G2 Bus Expansion Area is inhibited. (=> contention 3)

OK GD-DMA (GD => AICA Sound Memory)
NG GD-DMA (AICA sound memory => GD) <cannot be set>

(6.4) During GD-DMA (GD => G2 Bus Expansion Area), AICA reads are inhibited. (=> contention 4)

(6.5) Access by AICA-DMA is only allowed through System Memory => AICA Sound Memory, and Texture Memory => AICA Sound Memory. The only DMA mode allowed is the Interruptible, CPU Restart, and Empty Reference mode.

Accordingly, Register ADSTEL must be set to "0x00000005". (=> reference 3)

During AICA-DMA, AICA, access by program is inhibited. (=> contentions 5, 6)

OK AICA-DMA (System Memory => AICA Sound Memory) [ADTSEL=0x00000005]
OK AICA-DMA (Texture Memory => AICA Sound Memory) [ADTSEL=0x00000005]
NG AICA-DMA (AICA Sound Memory => System Memory) <cannot be set>
NG AICA-DMA (AICA Sound Memory => Texture Memory) <cannot be set>

Sound must be controlled and memory cycles must be left open for AICA sound memory so that program access (4-byte) to AICA is completed within 16 μ sec.

Restrictions on Multiple Access to the G2 Bus

There are 6 ways in which multiple access to the G2 Bus can result in errors. In all cases, the long access times that result can lead to errors in acquisition of Maple data or, in the worst case, inability to preserve system memory. (If this happens, access to the G2 Bus ends normally. Consequently, the pad may not work even though sound is normal.)
Be careful of the following: contentions 1, 3 and 6 when writing to AICA; contentions 2, 3, 4 and 5 when reading AICA, and contention 3 when accessing the G2 Bus.

(Contention 1) Writing to AICA by program

When writing to AICA by program, an error may occur if data previously written to AICA is present in the AICA write buffer.

[Countermeasure] When writing to AICA, use Register FFST and confirm that the AICA write buffer is empty. Defer the write until the write buffer is empty. (FFST Bit 0 => Reference 4)

Perform up to 8 writes to AICA at a time. For more than 8 writes, confirm that the write buffer is empty after every eight writes.

[Explanation] If the AICA write buffer is empty, no burden is imposed on the system for 8 or fewer writes because the write buffer holds 32 bytes (4 bytes x 8). For more than 8 writes, system operation will be interrupted for up to 16 μ sec (=>6.6).

(Contention 2) Reading AICA by program

When reading AICA by program, an error may occur if data previously written to the G2 Bus is present in either the Holly or AICA write buffer.

[Countermeasure] When reading AICA, use Register FFST and confirm that both the Holly and AICA write buffers are empty before doing the reads. (FFST Bits 5, 4, 0 => reference 4)

Once reading has commenced, it is not necessary to re-confirm that the write buffer is empty.

SH4 interrupts must be inhibited in order to prevent access from other SH4 routines.

[Explanation] AICA reads do not commence as long as data is present in the Holly CPUi/f Block or G2i/f Block write buffers.

(Contention 3) GD-DMA (GD => AICA Sound Memory) & G2 Bus access by program

GD-DMA (GD => AICA Sound Memory) is not possible concurrently with program access to the G2 Bus Control Register, MODEM, AICA or G2 Bus Expansion Area.

[Countermeasure] Wait until GD-DMA to AICA Sound Memory is completed before accessing the G2 Bus Control Registers, MODEM, AICA or G2 Bus Expansion Area by program.

For program writes to AICA Sound Memory, wait until GD-DMA is completed, then implement the contention 1 countermeasure.

When reading AICA by program, wait until GD-DMA to AICA Sound Memory is completed, then implement the contention 2 countermeasure.

[Explanation] When using GD-DMA (GD => AICA Sound Memory), the Holly G2i/f Block and the AICA write buffer are sporadically used for burst-write data. When there is burst-write data in both of these buffers, time is required to empty the G2i/f Block by writing the 32-byte data to AICA Sound Memory. This takes more than 16 μsec. Access to the G2 Bus takes even longer because it can only begin after G2i/f Block data is gone.

(Contention 4) GD-DMA (GD => G2 Bus Expansion Areas) & AICA reads by program

GD-DMA (GD => G2 Bus Expansion Area) is not possible concurrently with AICA reads by program.

[Countermeasure] Before reading AICA by program, wait for GD-DMA to the G2 Bus Expansion Area to end, then implement the contention 2 countermeasure.

[Explanation] When using GD-DMA (GD => AICA Sound Memory), the Holly G2i/f Block and the AICA write buffer are sporadically used for burst-write data. When AICA is read by program while there is burst-write data in the buffer, SH4 is stopped until the burst write to the G2i/f Block's G2 Bus Expansion Area and AICA read have been completed.

(Contention 5) AICA-DMA, EXT-DMA0, EXT-DMA1 & AICA reads by program

AICA reads by program are not possible concurrently with AICA-DMA, EXT-DMA0, or EXT-DMA1.

[Countermeasure] When reading AICA by program while AICA-DMA, EXT-DMA0, or EXT-DMA1 are in progress, suspend AICA-DMA, EXT-DMA0, and EXT-DMA1, verify that they are suspended, then implement the contention 2 countermeasure. DMA can be restarted after AICA has been read. (AICA-DMA, EXT-DMA0, EXT-DMA1 can be suspended and restarted as required.)

Alternatively, wait for AICA-DMA, EXT-DMA0, EXT-DMA1 to be completed, then implement the contention 2 countermeasure.

[Explanation] During AICA-DMA, EXT-DMA0, and EXT-DMA1, burst-write cycles occur sporadically on the G2 Bus. When this cycle occurs while AICA is being read by program, SH4 is stopped during the burst write on the G2 Bus and while AICA is being read.

(Contention 6) AICA-DMA & writing to AICA by program

AICA-DMA and writes to AICA by program are not possible concurrently.

[Countermeasure] When writing to AICA by program while AICA-DMA is in progress, suspend AICA-DMA, verify that it is suspended, then implement the contention 1 countermeasure. DMA can be restarted after writing to AICA has ended. (AICA-DMA can be suspended and restarted as required.)

Alternatively, the contention 1 countermeasure may be implemented after AICA-DMA has ended.

Examples of countermeasures for dual access to G2 Bus

[Contention 1 – countermeasure example 1] 8 writes to AICA

wait for the write buffer (AICA) to empty (FFST Bit 0)

⇩

8 writes to AICA by program

[Contention 1 – countermeasure example 2] 16 writes to AICA

wait for the write buffer (AICA) to empty (FFST Bit 0)

⇩

8 writes to AICA by program

⇩

wait for the write buffer (AICA) to empty (FFST Bit 0) <repeat contention 1– countermeasure 1>

⇩

8 writes to AICA by program

[Contention 2 – countermeasure example 1] Reading AICA

disable interrupts

⇩

wait for the write buffer (SH4i/f, G2i/f, AICA) to empty (FFST Bits 5, 4, 0)

⇩

read AICA by program

⇩

continue reading AICA by program as necessary

⇩

enable interrupts

[Contention 3 – countermeasure example 1] MODEM access during GD-DMA (GD => AICA Sound Memory)

wait for GD-DMA to end

⇩

access the MODEM by program

[Contention 3 – countermeasure example 2] 8 writes to AICA during GD-DMA (GD => AICA Sound Memory)

wait for GD-DMA to end

⇩

wait for the write buffer (AICA) to empty (FFST Bit 0)

<the remaining procedure is identical to contention 1 – countermeasure example 1>

⇩

8 writes to AICA by program

[Contention 3 – countermeasure example 3] 16 writes to AICA during GD-DMA (GD => AICA Sound Memory)

wait for GD-DMA to end

⇩

wait for the write buffer (AICA) to empty (FFST Bit 0)

<the remaining procedure is identical to contention 1 – countermeasure example 2>

⇩

8 writes to AICA by program

⇩

wait for the write buffer (AICA) to empty (FFST Bit 0)

⇩

8 writes to AICA by program

[Contention 3 – countermeasure example 4] Reading AICA during GD-DMA (GD => AICA Sound Memory)

wait for GD-DMA to end

⇩

disable interrupts <the remaining procedure is identical to contention 2 – countermeasure example 1>

⇩

wait for the write buffer (SH4i/f, G2i/f, AICA) to empty (FFST Bits, 5, 4, 0)

⇩

read AICA by program

⇩

continue reading AICA by program as necessary

⇩

enable interrupts

[Contention 4 – countermeasure example 1] Reading AICA during GD-DMA (GD => G2 Bus Expansion Area)

wait for GD-DMA to end

⇩

disable interrupts　　<the remaining procedure is identical to contention 2 – countermeasure example 1>

⇩

wait for the write buffer (SH4i/f, G2i/f, AICA) to empty　(FFST Bits 5, 4, 0)

⇩

read AICA by program

⇩

continue reading AICA by program as necessary

⇩

enable interrupts

[Contention 5 – countermeasure example 1] Reading AICA during EXT-DMA0 (when DMA is suspended)

disable interrupts (all access except SH4 access is inhibited)

⇩

suspend EXT-DMA0

⇩

confirm suspension of EXT-DMA0

⇩

wait for the write buffer (SH4i/f, G2i/f, AICA) to empty　(FFST Bits 5, 4, 0)

⇩

read AICA by program

⇩

continue reading AICA by program as necessary

⇩

resume EXT-DMA0

⇩

enable interrupts

[Contention 5 – countermeasure example 2] Reading AICA during EXT-DMA1 (when waiting for DMA to end)

wait for EXT-DMA1 to end

⇩

disable interrupts　　<the remaining procedure is identical to contention 2 – countermeasure example 1>

⇩

wait for the write buffer (SH4i/f, G2i/f, AICA) to empty　(FFST Bits 5, 4, 0)

⇩

read AICA by program

⇩

continue reading AICA by program as necessary

⇩

enable interrupts

[Contention 6 – countermeasure example 1] 8 writes to AICA during AICA-DMA (when DMA is suspended)

suspend AICA-DMA

⇩

confirm suspension of AICA-DMA

⇩

wait for the write buffer (AICA) to empty　　(FFST Bit 0)

⇩

8 writes to AICA by program

⇩

resume (AICAT?)-DMA

[Contention 6 – counter example 2] 16 writes to AICA during AICA-DMA (when waiting for DMA to end)

wait for AICA-DMA to end

⇩

wait for the write buffer (AICA) to empty　　(FFST Bit 0)

<the remaining procedure is identical to contention 1 – countermeasure example 2>

⇩

8 writes to AICA by program

⇩

wait for the write buffer (AICA) to empty (FFST Bit 0)

⇩

8 writes to AICA by program

(Reference)

(Reference 1) mapping of related items

G2 Bus Control Register	(A05F7800 - A05F78FF, A25F7800 - A25F78FF)
MODEM	(A0600000 - A06007FF, A2600000 - A26007FF)
AICA Register	(A0700000 - A0707FFF, A2700000 - A2707FFF, A0710000 - A0710007, A2710000 - A2710007)
AICA Sound Memory	(A0800000 - A09FFFFF, A2800000 - A29FFFFF)
G2 Bus Expansion Area	(01000000 - 01FFFFFF, 03000000 - 03FFFFFF, 14000000 - 17FFFFFF)
System Memory	(0C000000 - 0CFFFFFF, 0E000000 - 0EFFFFFF)
Texture Memory	(04000000 - 047FFFFF, 06000000 - 067FFFFF, 05000000 - 057FFFFF, 07000000 - 077FFFFF)

Access to the cache and store queue from the G2 Bus Control Register, MODEM and AICA is inhibited. The G2 Bus Expansion Area varies according to specifications of the connected hardware.

(Reference 2) Ways of accessing G2 Bus

*OK Accessing the G2 Bus Control Register with the SH4 program (4-byte access only)
*OK Accessing MODEM with the SH4 program (1-byte access only)
*OK Accessing AICA with the SH4 program (4-byte access only)
OK Accessing the G2 Bus Expansion Area with the SH4 program (possible when hardware is present)
*OK (only 1-, 2-, or 4- byte access is possible when no hardware is present)

*OK ... it is permitted with a restriction mentioned within ().

NG Accessing the G2 Bus Control Register by SH4 DMA (ch1, ch3) (inhibited)
NG Accessing the MODEM by SH4 DMA (ch1, ch3) (inhibited)
NG Accessing AICA by SH4 DMA (ch1, ch3) (inhibited)
OK Accessing the G2 Bus Expansion Area by SH4 DMA (ch1, ch3) (possible when hardware is present)
NG (inhibited when no hardware is present)

OK GD-DMA (GD => G2 Bus Expansion Area)
OK GD-DMA (GD => AICA Sound Memory)
NG GD-DMA (G2 Bus Expansion Area => GD) <inhibited>
NG GD-DMA (AICA Sound Memory => GD) <inhibited>
OK AICA-DMA (System Memory => AICA Sound Memory)
OK AICA-DMA (Texture Memory => AICA Sound Memory)
NG AICA-DMA (AICA Sound Memory => System Memory) <inhibited>
NG AICA-DMA (AICA Sound Memory => Texture Memory) <inhibited>
OK EXT-DMA1 (System Memory => G2 Bus Expansion Area)
OK EXT-DMA1 (Texture Memory => G2 Bus Expansion Area)
OK EXT-DMA1 (G2 Bus Expansion Area => System Memory)
OK EXT-DMA1 (G2 Bus Expansion Area => Texture Memory)
OK EXT-DMA2 (System Memory => G2 Bus Expansion Area)
OK EXT-DMA2 (Texture Memory => G2 Bus Expansion Area)
OK EXT-DMA2 (G2 Bus Expansion Area => System Memory)
OK EXT-DMA2 (G2 Bus Expansion Area => Texture Memory)

Other types of DMA to the G2 Bus are not possible.
Refer to the SH4 specifications for restrictions on using SH4 ch1-DMA and ch3-DMA.

(Reference 3) Registers that control DMA operations for AICA-DMA, EXT-DMA1 and EXT-DMA2

The DMA control registers provide DMA suspend enable bits, DMA trigger selection bits, and external hardware write buffer empty status bits.

ADTSEL (A05F7810) AICA-DMA trigger selection register
E1TSEL (A05F7830) Ext-DMA1 trigger selection register
E2TSEL (A05F7850) Ext-DMA2 trigger selection register
bit2: DMA suspend (0: disable /1:enable) <setting to 0 is inhibited>
bit1: trigger select (0: CPU triggered/1: interrupt triggered)
bit0: write buffer empty (0: not referenced/1: referenced)

(Reference 4) SH4 can check the status of the hardware's internal write buffers by referring to register FFST

FFST (A05F688C) FIFO status register
bit5: Holly CPUi/f Block internal write buffer (0: empty/1:data present)
bit4: Holly G2i/f Block internal write buffer (0: empty/1:data present)
bit3: undefined
bit2: undefined
bit1: undefined
bit0: AICA internal write buffer (0: empty/1: data present)

This register can be accessed freely because it is not located on the G2 Bus.